What is claimed is:

1. A shared memory multiprocessor comprising:

a plurality of nodes each configured with at least one of a processor having a cache memory, a memory device and an I/O device, and a node controller; and

an inter-node connection network for interconnecting a plurality of said nodes;

wherein at least one of a plurality of said nodes includes said processor and at least one of said memory device and said I/O device, and the whole of a plurality of said nodes include at least one said processor, at least one said memory device and at least one said I/O device;

wherein said node controller of each of a plurality of said nodes includes a processor unit constituting an interface with said processor in a local node, at least a memory unit constituting an interface with said memory device in the local node and an I/O unit constituting an interface with said I/O device in the local node, a network unit constituting an interface with said inter-node connection network, and an intra-node connection circuit for connecting said processor unit and at least one of said memory device and said I/O device to said inter-node connection network unit;

wherein said processor unit includes an inter-unit address decode circuit and a cache coherence control circuit,

said inter-unit address decode circuit decoding the control information and the address information in a memory access request or an I/O access request issued by the processor in the local node, and adding to said access request the information on the node associated with the memory unit or the I/O unit intended as a destination of said access request, the information on the unit intended as a destination of said access request, and the cache coherence control information indicating whether the cache coherence control is required or not,

said cache coherence control circuit performing the cache coherence control of the processor in the local node in the case where the cache coherence control information added to the access request received from said network unit indicates that the cache coherence control is required;

wherein said I/O unit includes an inter-unit address decode circuit whereby the node information and the unit information for the memory unit or the I/O unit intended as a

access request destination and the cache coherence control information indicating whether the cache coherence control is required or not are added to the memory access request or the I/O access request issued by the I/O device in the local node;

wherein said network unit includes a transfer unit for transferring the access request received from said intra-node connection circuit to said inter-node connection network, and a transfer unit for transferring the access request transferred thereto from said inter-node connection network to said intra-node connection network;

wherein said intra-node connection circuit transfers said access request to the unit in the local node designated as a destination of transfer based on the cache coherence control information, the node information and the unit information added to the access request transferred from said inter-node connection network through said network unit; and

wherein said inter-node connection network transfers said access request to the node designated by the cache coherence control information and the node information added to the access request received from said network unit.